# Application Note 171

Using M8051EW Memory Extension

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This Application Note tells you how to configure the Keil 8051 development tools for Mentor M8051EW based devices with integrated Memory Extension. With this Memory Extension it is possible to access up to 1MByte code and data space.

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## Overview

Some 8051 devices that are based on the M8051EW core offer a set of Memory Extension registers (MEX1, MEX2 and MEX3) that support an extended code and data memory space of up to 1 Mbyte.

**NOTE:** *M8051EW Memory Extension registers are fully supported by PK51 Version 7.50 or higher. This version provides also full device simulation for the Memory Extension registers.*

### Program Code Extension

Program Code is always fetched from the 64K block pointed to by a Current Bank value (CB). CB is updated from the Next Bank value (NB) upon execution of long jump (LJMP) and call (LCALL, ACALL) instructions. The MEX1 register contains NB (MEX1.3 - MEX1.0) and CB (MEX1.7 - MEX.4). An extra Memory Extension Stack space is used to save and restore the MEX1 register on call (LCALL, ACALL) and return (RET, RETI) instructions. Interrupt service routines are always executed from code in the 64K block pointed to by the Interrupt Bank value (IB) (MEX2.3 - MEX2.0).

The program code extension of the M8051EW core is supported with the **IBANKING** linker control that is available in the BL51 Linker/Locater and the LX51 Linker/Locater.

### Constant and Data Memory Extension

Constant and Data Memory can be extended with additional fields in the Memory Extensions registers. The Memory Constant Bank pointer (MCB) (MEX3.7, MEX2.6 - MEX2.4) is enabled with the MCM bit (MEX2.7) and defines a 64KB memory bank that is used for constants that are defined with the C51 memory type **code**. The Memory XRAM Bank pointer (MX) (ME3.4, MEX3.2 - MEX3.0) is enabled with the MXM bit (MEX3.3) and defines a 64KB memory bank that is used for variables that are defined with the C51 memory type **far**.

Constant and Data Memory Extension is only supported with the LX51 Linker/Locater and is therefore only available in the Keil PK51 Professional Developers Kit. The bank used for constant and the number of xdata banks is configured in the **L51IBANK.A51** file that is part of this Application Note.

## IBANKING Linker/Locater Control

With the linker/locater control **IBANKING** the linker uses the on-chip code banking hardware of the M8051EW devices. The linker/locater places automatically all code segments in the bank area, which do not have the ?CO? prefix or ?CO postfix. Segments with a ?CO prefix or postfix are placed into the common area.

Interrupt Functions and the startup code must be located to the code bank 0 which is the IB reset value.

The standard bank configuration module L51\_BANK.A51 is not required when the control **IBAKING** is used. Instead the linker/locater generates in this operation mode a jump table with the following format:

MOV MEX1,#BANK\_NUMBER  
 LJMP target

The IBANKING control is entered in uVision2 under **Options - Lx51 Misc - Misc Controls**.

**NOTE:**

* Program code banking with Mentor M8051EW devices requires special C51 run-time libraries. These C51 run-time libraries have the name format **C51M\*.LIB** and are automatically added when using the Linker/Locator control **IBANKING.**

## L51IBANK.A51 Memory Extension Configuration File

The **L51IBANK.A51** file allows configuration of both program code and variable banking. You can specify a separate code memory bank used for program constants and the memory bank used for interrupt functions.

When using this configuration file it is possible to use up to:

* up to 16 x 64KB banks for program code
* fixed 64KB bank for constants defined with the memory type **code**
* fixed 64KB bank for variables defined with the memory type **xdata**
* up to 8 x 64KB banks for variables defined with the memory type **far** (for support of 16 banks, the macro LOAD\_BANK requires adaption)

The **L51IBANK.A51** configuration file is only supported with the LX51 Linker/Locater and is therefore only available in the Keil PK51 Professional Developers Kit. The constant variable bank, interrupt code bank, and the far variable banks are configured in the **L51IBANK.A51** file. The Linker/Locater control **IBANKING** is not required when you are using the **L51IBANK.A51** configuration file.

**NOTE:**

* The C51 Compiler must be invoked with the directive **VARBANKING(1)** when you are using the **L51IBANK.A51** configuration file. In uVision2 this directive is specified under **Options for Target - Target - 'far' memory type support** and **Options for Target - Target - Save address extension SFR in interrupts.** The C51 run-time libraries **C51N\*.LIB** and are automatically added when far memory support is selected.

### Optimum Bank Layout with L51IBANK.A51 Configuration File

The following design rules help you to get optimum results when you are using the L51IBANK.A51 configuration file.

* You may use a **?B\_CB** value in the L51IBANK.A51 configuration file to define a single 64KB bank for constants. In this way the constants are not copied into the common bank.
* For complex switch/case statements the C51 compiler generates intrinsic function calls (?C?CCASE, ?C?ICASE, or ?C?LCASE) that embed constants into program code. If a constant bank is defined with the **?B\_CB** value, the LX51 Linker/Locater automatically relocates such functions into the common area. These relocations are listed in the Linker/Locater MAP file under the section **FUNCTION CONTAINING SPECIAL LIB CALLS RELOCATED TO COMMON**. You can avoid function relocation to the common area in two ways:
  1. Locate modules that are using the intrinsic functions ?C?CCASE, ?C?ICASE, or ?C?LCASE into the same code bank defined for constants with the **?B\_CB** value.
  2. Optimizing the program code as explained under [C51: SWITCH/CASE STATEMENTS](http://www.keil.com/support/docs/1316.htm) or split the switch/case into several smaller switch/case statements.
* Modules that contain interrupt functions should be located to the code bank defined interrupt bank with the **?B\_IB** value. For such interrupt functions, the LX51 Linker/Locater does not generate any bank switch code.

## Simulation of Mentor M8051EW Features

The CPU Core Simulation DLL **S8051.DLL** provides additional parameters for the extended features of the M8051EW core. These parameters can be stored in the DeviceDatabase� or may be entered under **Options - Debug - Simulator CPU DLL Parameter**:

* **-m8051EW** changes the behavior of the opcode 0xA5 to **MOVC @(DPTR++),A** and enables the multiple DPTR registers. The simulator is expanded with the EO register that is located by default at SFR address 0xA2.
* **-eNN** selects the SFR address of the EO register. Example: **-e93**
* **-mex** enables the MEX1 (SFR 0x94), MEX2 (SFR 0x95), MEX3 (SFR 0x96), and MEXSP (SFR 0x97) memory extension registers. Depending on the settings of these memory extension registers, the MOVX and MOVC instruction will use the extended address range. Also these registers are used for code memory address banking. The memory expansion stack is simulated in the memory type S:. You may view the content of the extension stack using the memory window in the address range S:0 - S:0x7F.

## Compiler Support of Multiple DPTR

The Mentor M8051EW Core can be configured to support 2, 4, or 8 DPTR registers. The multiple DPTR registers are identical to [Infineon Devices](http://www.keil.com/support/man/docs/c51/c51_dv_infineondataptr.htm), however the DPSEL register is located at address 0xA2. The DPSEL SFR location can be configured by using the following assembly statements:

PUBLIC ?C?DPSEL  
?C?DPSEL DATA 0A2H

This configures the DPSEL register address for the C51 library functions memcpy, memcmp, memmove, strcpy, and strcmp.

**Notes:**

* The **L51IBANK.A51** file contains already a definition for the ?C?DPSEL register.
* For device simulation the ?C?DPSEL setting must be identical with the **-eNN** configuration string.

## Example Programs

Example programs in the folder **..\C51\EXAMPLES\M8051EW** demonstrate to usage of the Memory Extension on M8051EW based devices. The examples show the configuration of the uVision2 IDE. The programs can be fully simulated with the uVision2 Debugger.

## Restrictions with RTX51

Program code banking with the Mentor M8051EW Memory Extension registers is not supported by RTX51 Full or RTX51 Tiny, since it is not possible to access the Memory Extension Stack space.

## Technical Support

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## Contact Details

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| **In the USA...**  **Keil - An ARM Company**  1501 10th Street, Suite 110  Plano, TX  75074  USA  800-348-8051 - Sales  972-312-1107 - Support  972-312-1159 - Fax  [sales.us@keil.com](mailto:sales.us@keil.com) - Sales E-Mail  [support.us@keil.com](mailto:E-Mailsupport.us@keil.com) - Support E-mail |  | **In Europe...**  **Keil - An ARM Company**  Bretonischer Ring 15  D-85630 Grasbrunn  Germany  +49 89 456040-0 - Sales  +49 89 456040-24 - Support  +49 89 468162 - Fax  [sales.intl@keil.com](mailto:sales.intl@keil.com) - Sales E-Mail  [support.intl@keil.com](mailto:E-Mailsupport.intl@keil.com) - Support E-Mail |
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